FIG. 1

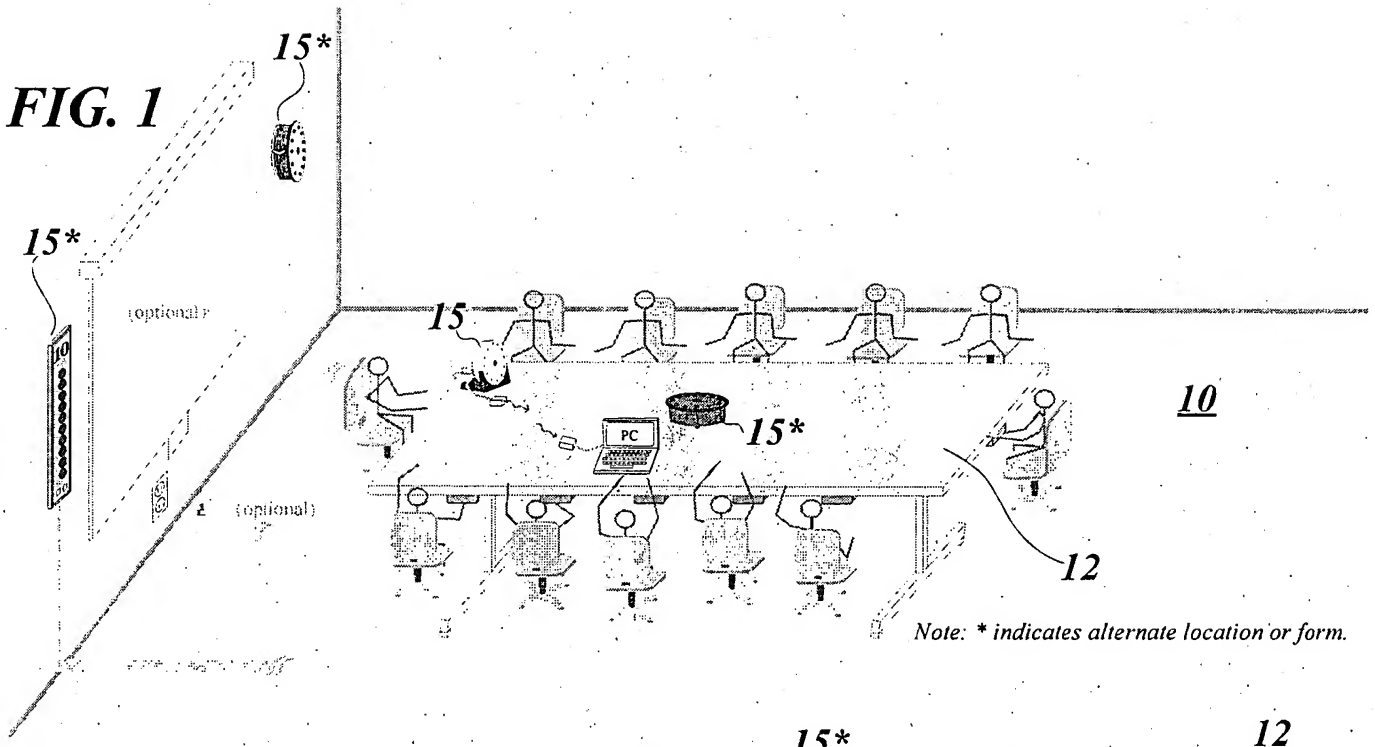


FIG. 2

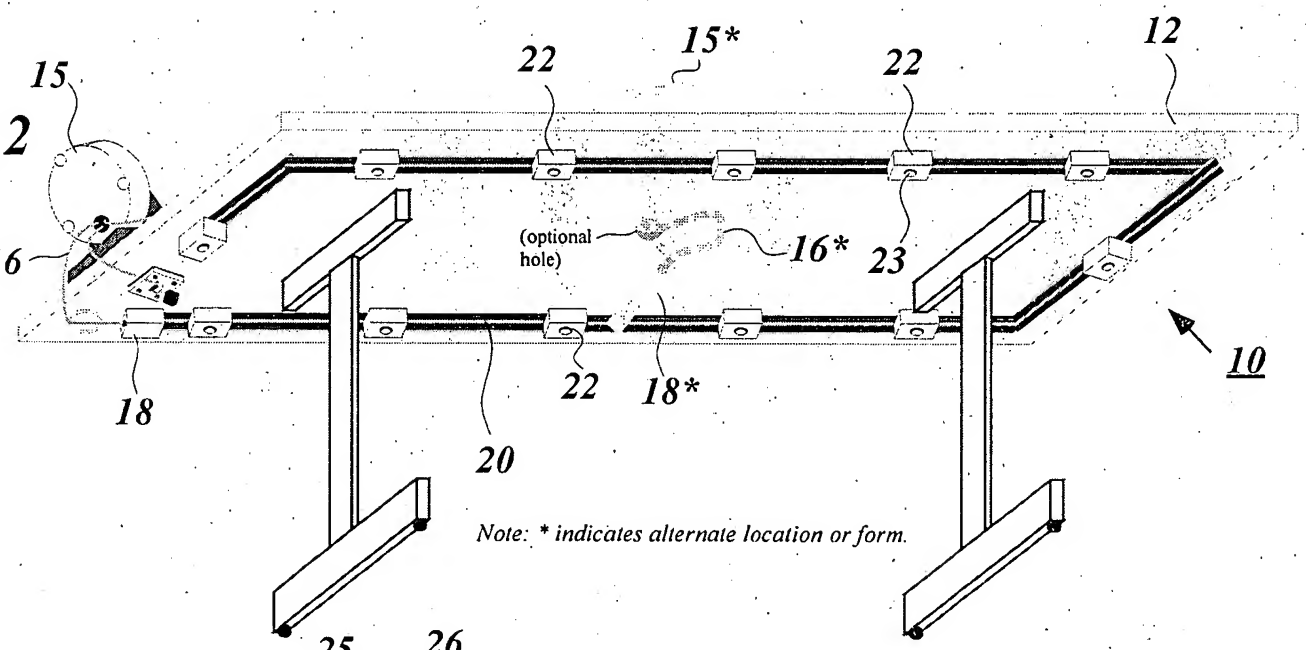
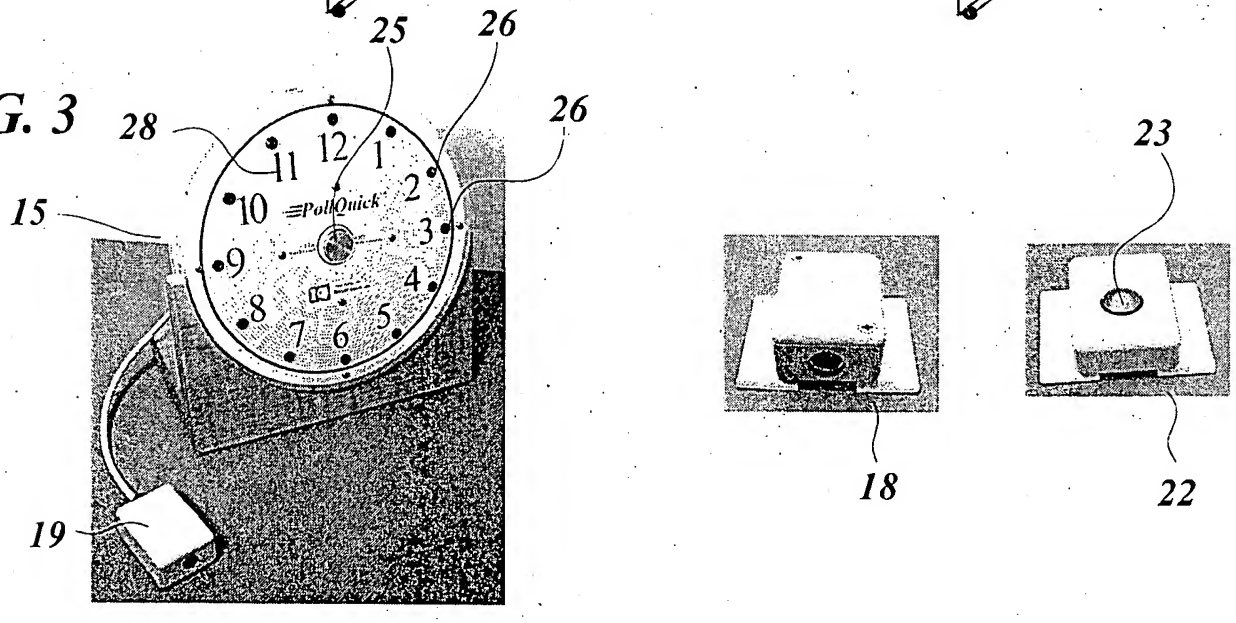


FIG. 3



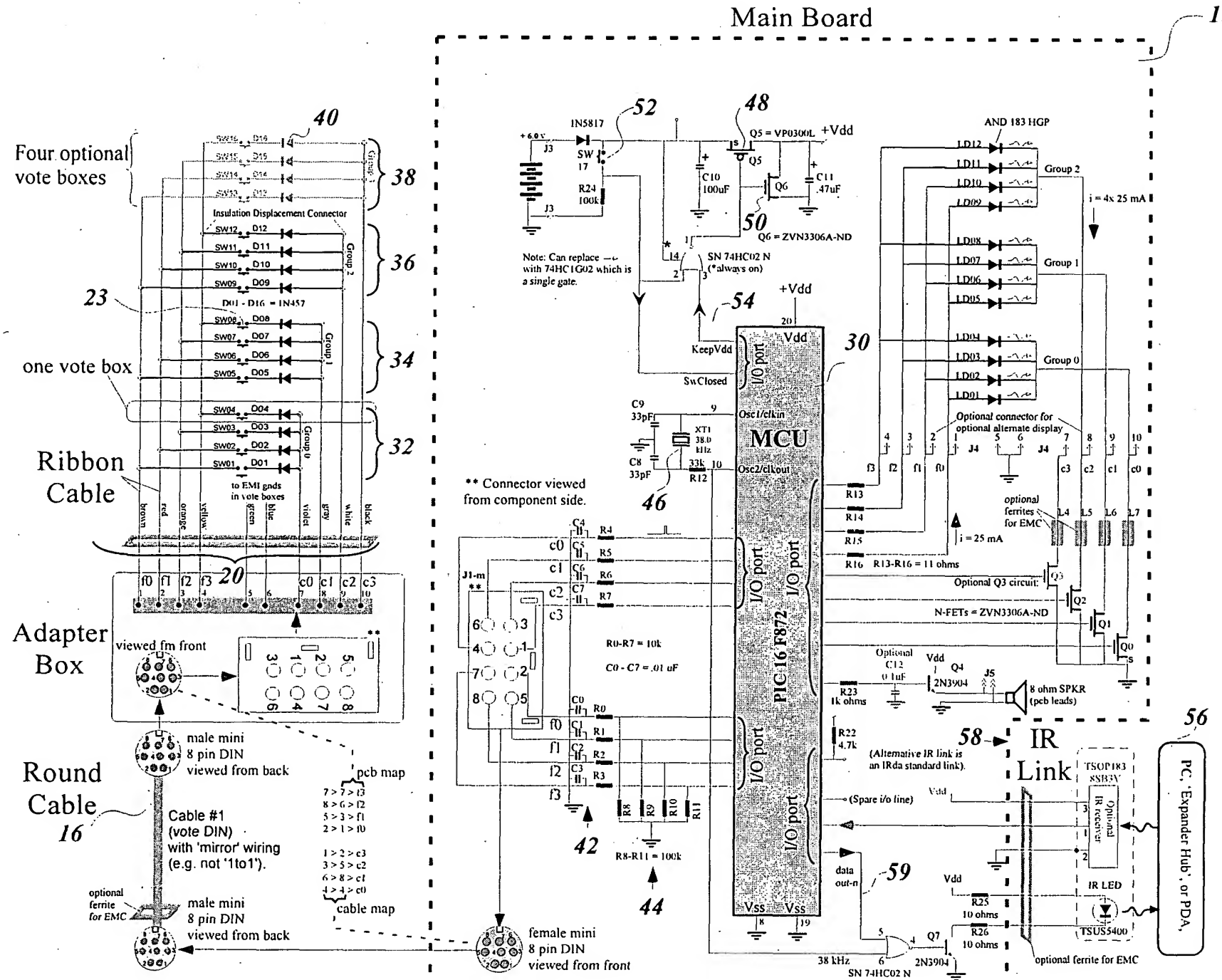

Main Board
15
Four optional vote boxes
40
38
36
34
32
23
one vote box
Ribbon Cable
Insulation Displacement Connector
D01 - D16 = 1N457
to EMI gnds in vote boxes
brown
red
orange
yellow
green
blue
violet
gray
white
black
20
Adapter Box
viewed fm front
male mini 8 pin DIN viewed from back
Round Cable
16
Cable #1 (vote DIN) with 'mirror' wiring (e.g. not '1to1').
optional ferrite for EMC
male mini 8 pin DIN viewed from back
pcb map
cable map
female mini 8 pin DIN viewed from front
** Connector viewed from component side.
52
48
1N5817
Q5 = VP0300L
+Vdd
SW 17
R24 100k
C10 100uF
C11 .47uF
Q6
50
Q6 = ZVN3306A-ND
Note: Can replace with 74HC1G02 which is a single gate.
SN 74HC02 N (*always on)
54
KeepVdd
SwClosed
30
MCU
PIC16F872
I/O port
Osc1/clkin
Osc2/clkout
C9 33pF
C8 33pF
XT1 38.0 kHz
33k R12
46
R0-R7 = 10k
C0 - C7 = .01 uF
R8-R11 = 100k
42
44
AND 183 HGP
Group 2
Group 1
Group 0
i = 4x 25 mA
Optional connector for optional alternate display
optional ferrites for EMC
i = 25 mA
R13-R16 = 11 ohms
Optional Q3 circuit:
N-FETs = ZVN3306A-ND
Optional C12 0.1uF
R23 1k ohms
Q4 2N3904
J5
8 ohm SPKR (pcb leads)
R22 4.7k
(Alternative IR link is an IRda standard link).
58
IR Link
56
PC, 'Expander Hub', or PDA,
TSOP183 8SB3V
IR receiver
Optional
IR LED
TSUS5400
optional ferrite for EMC
(Spare i/o line)
data out-n
59
R25 10 ohms
R26 10 ohms
Q7 2N3904
38 kHz
SN 74HC02 N

FIG. 4A

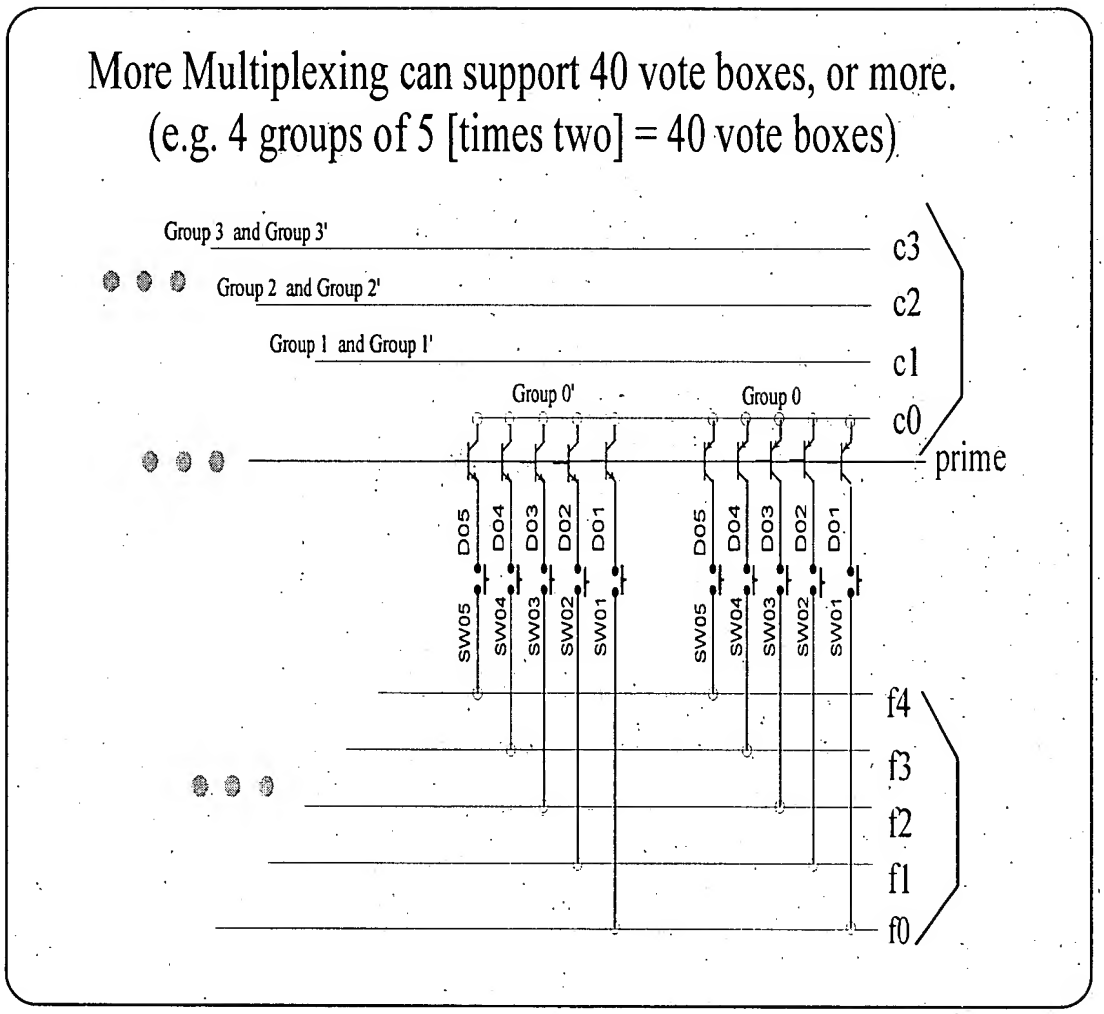

More Multiplexing can support 40 vote boxes, or more.
(e.g. 4 groups of 5 [times two] = 40 vote boxes)
Group 3 and Group 3'
Group 2 and Group 2'
Group 1 and Group 1'
Group 0'
Group 0
c3
c2
c1
c0
prime
D05
D04
D03
D02
D01
SW05
SW04
SW03
SW02
SW01
f4
f3
f2
f1
f0

FIG. 4B

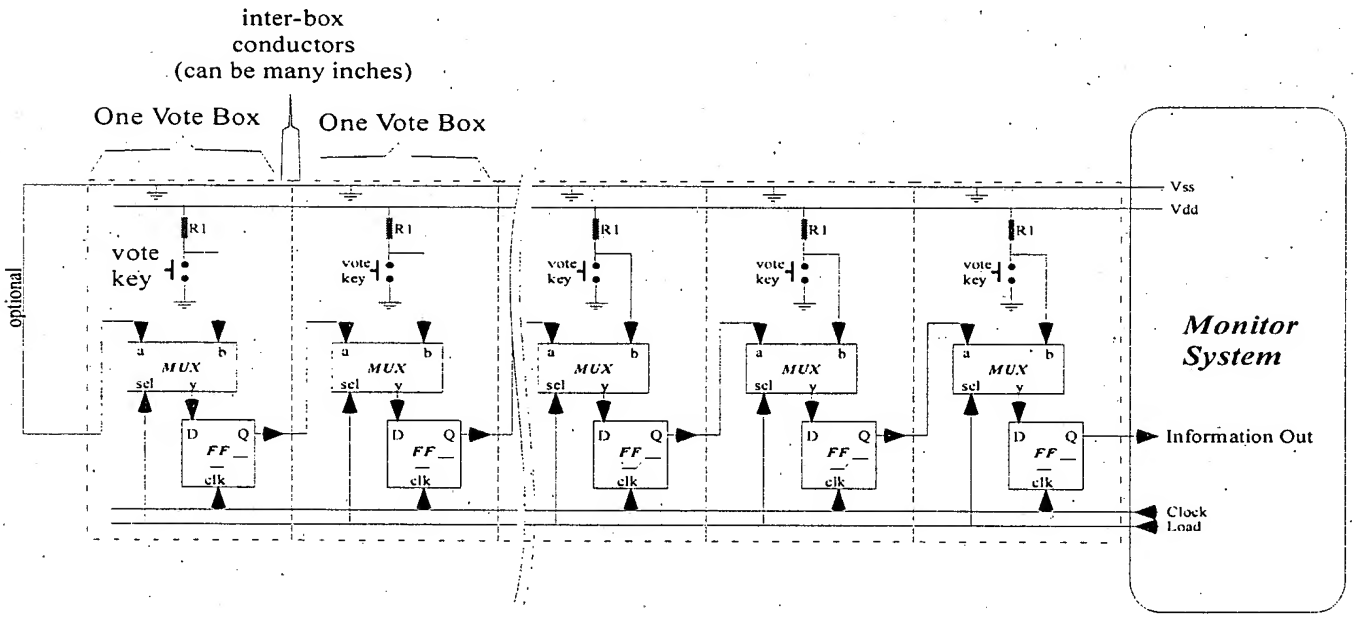
A Shift Register Version

Pros:

1. Can extend to large number of (identical) vote boxes.
2. All vote boxes are identical.
3. Data out (each Q) drives only small loads.

Cons:

1. Logic (ICs) required in each vote box.
2. Power (Vdd, Vss) must be supplied to the ICs.
3. More than 2 contacts per votebox are critical.
4. The clock drives multiple loads (unless made asynchronous).
5. Slow data out for given clock frequency (unless parallel paths used. See 3 below).
6. More FCC noise issues.
7. Press-on tool is more complicated (added cutting mechanism) since one or more conductors must be segmented.



Note: Simple refinements are possible:

1. We can supply Vdd (for FF & Mux) via the clock (rectified & LP filtered).
2. We can reduce the number of inter-box conductors by encoding "load" (for example) on other conductors. Even just 2 conductors can suffice.
3. More conductors can be used to simultaneously send several bits.
4. A 'counters with digital comparitors' approach could replace the 'shift register' (above) approach.

FIG. 4C

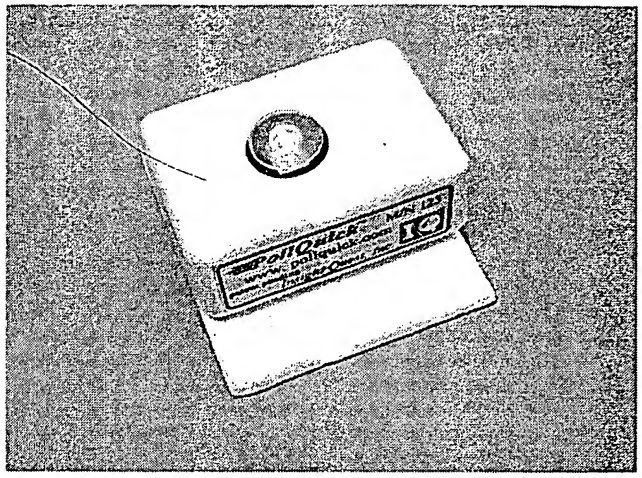


FIG. 5

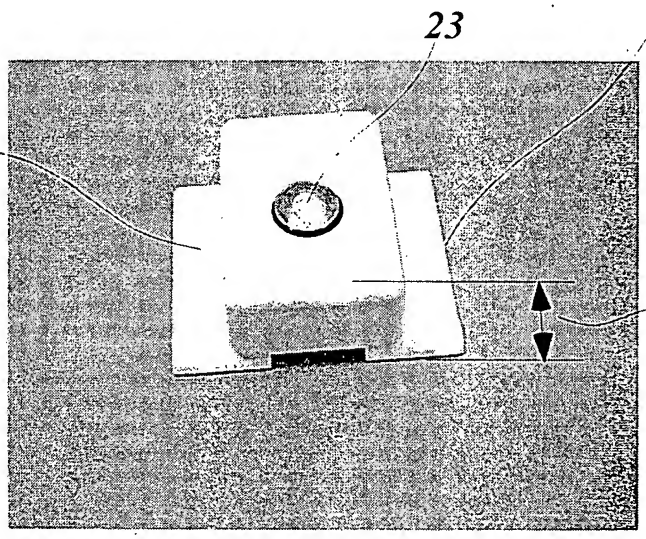


FIG. 6

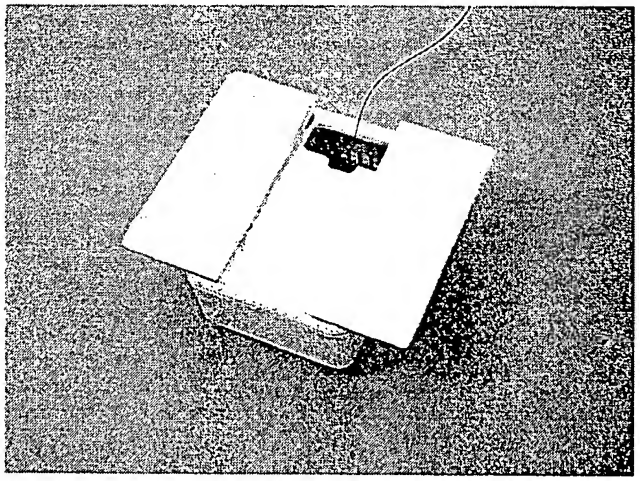


FIG. 7

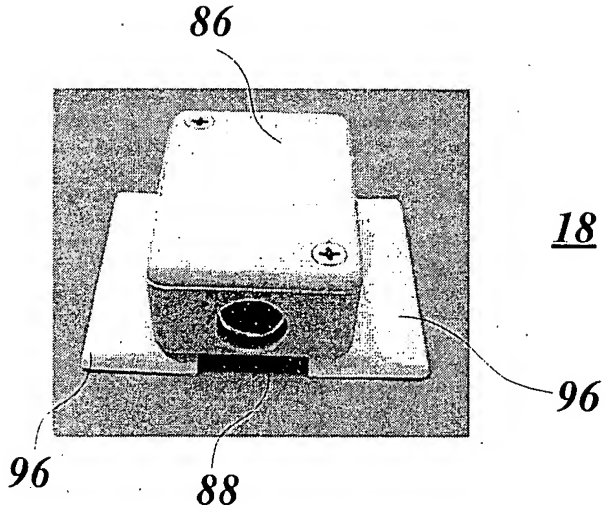


FIG. 8

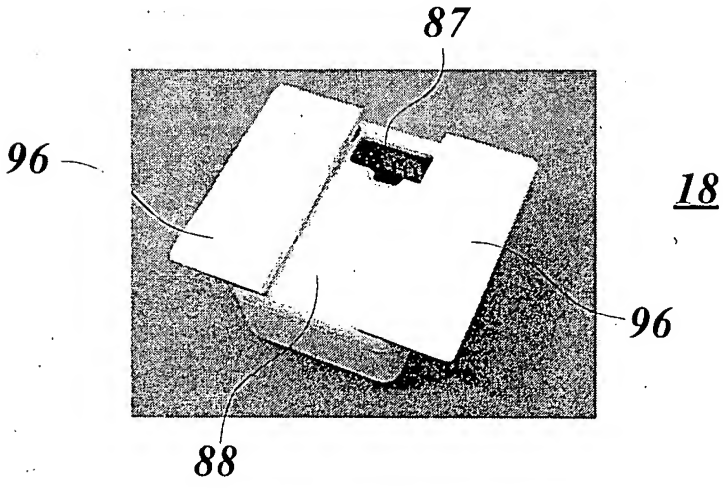


FIG. 9

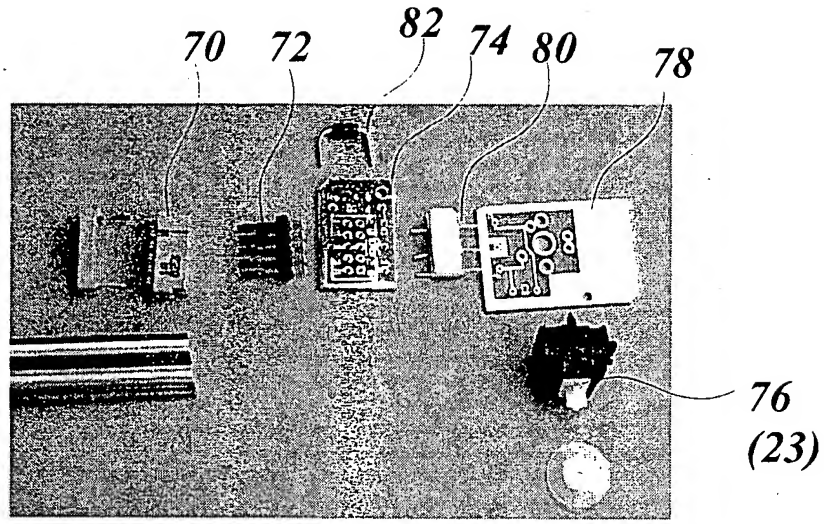


FIG. 10

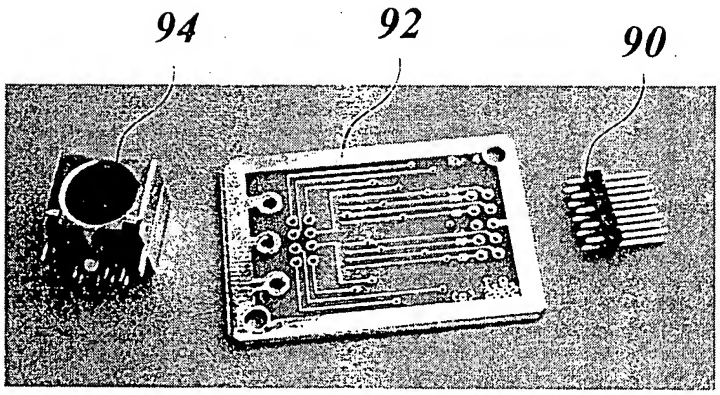


FIG. 11

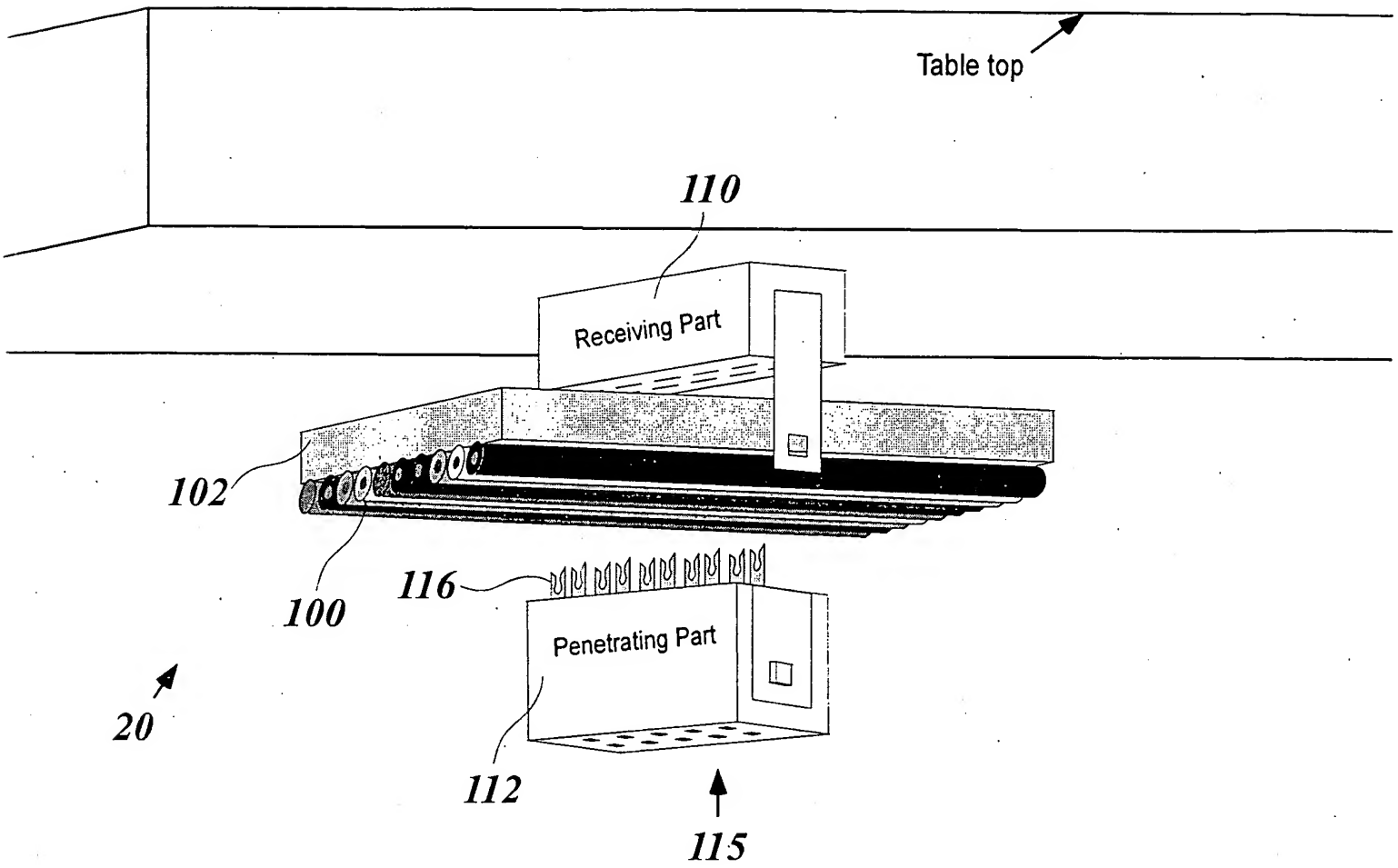


Table top
110
Receiving Part
102
100
116
Penetrating Part
20
112
115

FIG. 12

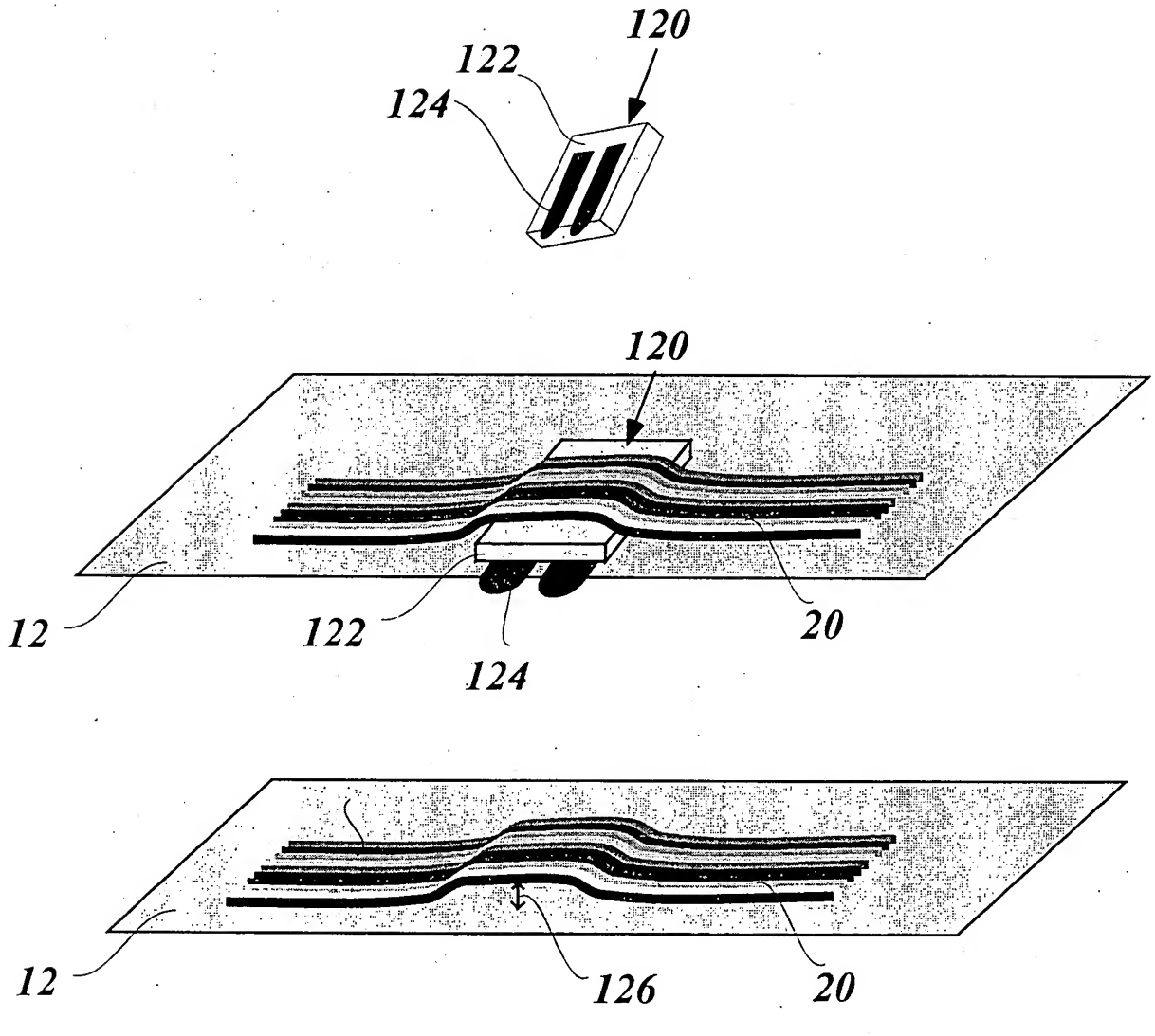


FIG. 13

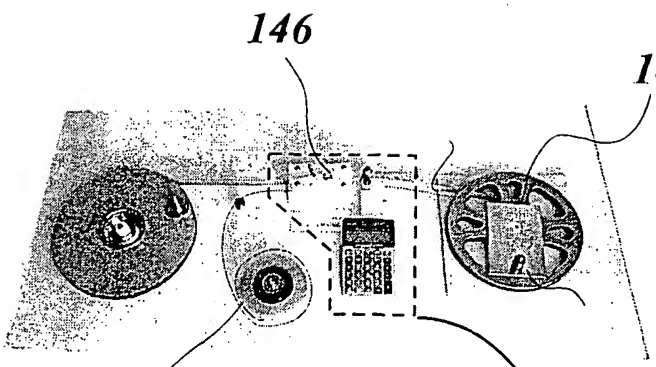


FIG. 14

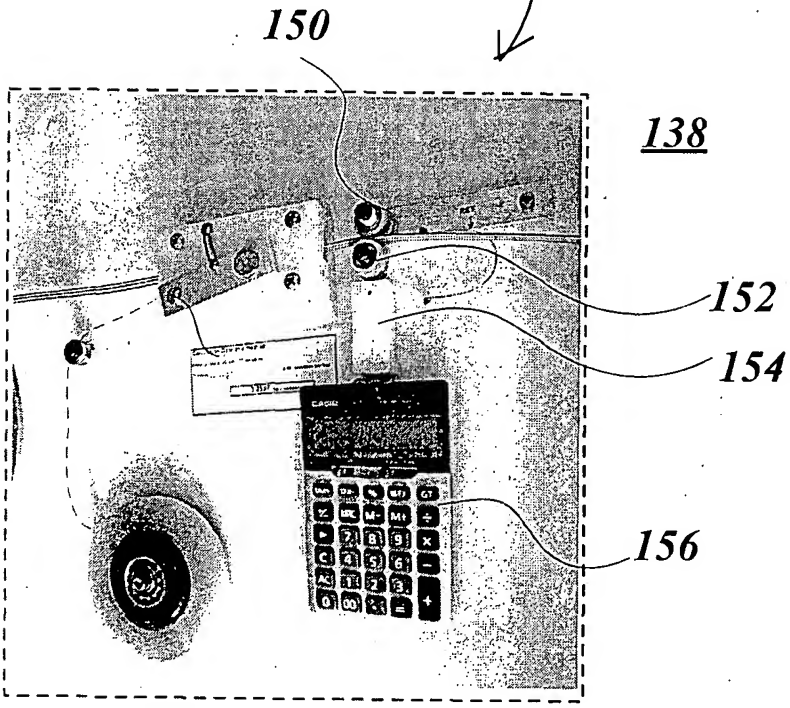


FIG. 15